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STIRLING et al

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January 15, 2004

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

SUBMISSION OF PRIORITY DOCUMENTS

It is respectfully requested that this application be given the benefit of the foreign filing date under the provisions of 35 U.S.C. §119 of the following, a certified copy of which is submitted herewith:

Application No.	Country of Origin	Filed
9703216.3	Great Britain	17 February 1997
9704901.9	Great Britain	10 March 1997
9710908.6	Great Britain	27 May 1997
9716083.2	Great Britain	30 July 1997
9719415.3	Great Britain	12 September 1997
9721170.0	Great Britain	7 October 1997

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: Larry S. Nixon

Larry S. Nixon
Reg. No. 25,640

LSN:vc
1100 North Glebe Road, 8th Floor
Arlington, VA 22201-4714
Telephone: (703) 816-4000
Facsimile: (703) 816-4100

USSN
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Request for grant of a patent

The Patent Office
Cardiff Road
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Gwent NP9 1RH

1. Your Reference
47/62787GB

2. Patent Application No
9719415.3 12 SEP 1997

3. Full name, address and postcode of the or of each applicant (*underline all surnames*)

Communication & Control Electronics Limited
Stirling House
Stirling Road
The Surrey Research Park
Guildford, Surrey GU2 5RF

6791636002

Patents ADP number (*if known*)

If the applicant is a corporate body, give the country/state of its incorporation — Country: United Kingdom
State:

4. Title of the invention
LOCAL COMMUNICATION SYSTEM

5. Name of Agent
FITZPATRICKS

"Address for Service" in the United Kingdom to which all correspondence should be sent
4 West Regent Street
Glasgow
G2 1RS

Patents ADP number
00000695002

6. Priority Details

Country	Priority Application Number	Date of filing
GB	9703216.3	17 February 1997
GB	9704901.9	10 March 1997

7. If this application is divided or otherwise derived from an earlier UK application give details

Number of earlier application	Date of filing
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Patents form 1/77

8. Is a statement of inventorship and or right to grant of a patent required in support of this request?:

9. Enter the number of sheets for any of the following items you are filing with the form.

Continuation Sheet for this form	0
Description	18
Claims	0
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Priority documents	-
Translations of priority documents	-
Statement of inventorship and right to grant of a Patent (*Patents Form 7/77*)	-
Request for Preliminary examination and search (*Patents form 9/77*)	-
Request for Substantive Examination (*Patents Form 10/77*)	-

11. I/We request the grant of a patent on the basis of this application

Signature FITZPATRICKS Date: 12 September 1997

12. Name and daytime telephone number of person to contact in the United Kingdom

John James GRAY

0141 306 9000

LOCAL COMMUNICATION SYSTEM

The invention relates to a local communication system wherein plural stations are connected in a ring topology. The invention provides a novel local communication system, and stations and interface components for use in such a system.

A local communication system which combines source data (CD audio, MPEG video, telephone audio etc) with control messages in a low cost fibre network has been proposed in the form of D2B Optical. For details, see for example the "Conan Technology Brochure" and the "Conan IC Data Sheet" available from Communication & Control Electronics Limited, Stirling House, Stirling Road, The Surrey Research Park, Guildford, Surrey, GU2 5DR (also http://www.candc.co.uk). See also German patent applications of Becker GmbH with filing numbers 19503206.3 (95P03), 19503207.1 (95P04), 19503209.8 (95P05), 19503210.1 (95P06), 9503212.8 (95P07), 19503213.6 (95P08), 19503214.4 (95P09) and 19503215.2 (95P10). "Conan" is a registered trade mark of Communication & Control Electronics Limited.

The present invention aims to enable expansion of the capacity of such a network, for use in vehicles and the like, while maintaining compatibility with existing D2B Optical Products and designs. The invention is nevertheless applicable in systems other than D2B Optical, where different components may operate at different speeds.

According to one aspect of the invention, there is disclosed a local communication system comprising a ring network, the data rate in a first segment of the ring being higher than that in a second segment of the ring.

Synchronisation may be maintained for example by the provision of a regular frame structure which has the same frame period in both segments of the network, but a larger quantity of data in each frame of the first segment.

In a network where each segment of the ring conveys one or more channels of user information at a relatively high data rate, and one or more channels of control information, the data rate for control information may be constant between the first and second segments, while the data rate for user information is different.

Depending on the distribution of source and destination stations around the ring, the user information flowing in the second segment may be a subset of that flowing in the first segment of the network.

It will be appreciated that stations in the second segment of the network may for example implement the existing D2B Optical protocols, and hence exploit existing product designs. The stations in the first segment of the ring can employ a novel transceiver adapted to the higher data rates. The transceiver disclosed can provide the necessary buffering and switching of user information to interface between the two segments of the network operating at different rates.

In the proposed embodiment, the frame rate is constant in each segment around the network, and within each frame the same number of bits are reserved to form the control message channel in every segment. The control frame format is thus continuous around the ring. On the other hand, the number of user information ("source data") bits included in each frame is higher in the first segment of the network, and the bit rate in the optical fibre or other channel is much higher than in the second segment. By this means, the provision of higher data capacity does not require a development of new

protocols and communication management software for control messages, but only minor adaptation to allow control of a more versatile user information channels.

Embodiments of the invention will now be described, by way of example only, with reference to the accompanying drawings, in which:

Figure 1 shows in block schematic form a known local communication system embodying the D2B Optical system;

Figure 2 illustrates the control and source data architecture used in the system of Figure 1;

Figure 3 represents a station with integral interface;

Figure 4 schematically illustrates one of the interface modules of Figure 1;

Figure 5 shows the frame structure of digital signals transmitted according to the known D2B Optical format between the apparatuses in the system of Figure 1;

Figure 6 shows the sub-frame structure of digital signals transmitted according to the known D2B Optical format between the apparatuses in the system of Figure 1;

Figure 7 is a functional block diagram of a network transceiver IC according to the present invention;

Figure 8 shows the frame structure of digital signals transmitted according to the novel D2B Optical Plus format using the transceiver of Figure 7;

Figure 9 shows a first sub-frame format in the system of Figure 8;

Figure 10 shows a second sub-frame format in the system of Figure 8;

Figure 11 shows a control frame format common to the systems of Figures 1 and 8;

Figure 12 shows schematically a ring network incorporating different formats in different segments using the transceiver of Figure 7;

Figure 13 and 14 illustrate source data routing in the transceiver of Figure 7.

Background

The known system illustrated in Figure 1 comprises nine audio- or video-related apparatuses 101-109 connected as stations (or nodes) of a Local Area Network (LAN). Of course more or fewer than nine stations may be accommodated. In this example system, the apparatuses are: a control and display unit 101, a Compact Disc memory (CD-ROM) reader 102, a radio turner 103, a CD changer unit 104, an audio power amplifier 105, a facsimile send/receiver unit (FAX) 106, a video recording system (VCR/CAMCORDER) 107, a video tuner 108, and a telephone 109. The display function of the control and display unit 101 may for example provide for display of information read from memory devices by CD-ROM and/or display of video signals from tuner 108 or VCR 107.

The LAN interconnection in the known system comprises nine unidirectional point-to-point fibre optic links 111-119 linking interface modules 121-129, each of which is substantially structurally identical, such that the nodes are all connected in a ring. Each fibre optic link carries a combination of digital audio/video signals, CD-ROM data and control messages in accordance with a signal frame structure to be described in detail below. A designated station (referred to hereinafter as

the system master), such as the control/display unit 101, continuously generates the frame structure at a frame sample rate of 20-50kHz (typically 44.1kHz as for CD sampling). One station on the network is designated to act as system master on power-up although the role of system master may subsequently be re-allocated to another station, for example in fault conditions.

The data architecture of a station's interface to the fibre optic ring is schematically illustrated in Figure 2. From the ring 119-111, a media access control (MAC)/physical layer 300 (to be described in greater detail hereinafter) together with a communications management layer 302 for control messages are provided in interface module 121. The communications management layer 302 manages address initialisation and verification and ensures the reliable transport of messages by retransmission according to defined timing rules. Data handling for source data 304 and application protocols for control messages 306 are provided at station level 101, with the application protocols typically defining a device/subdevice grouping and control hierarchy for the station, the format of information exchanged between products, the behaviour of devices/subdevices, and application level timing. It will be readily understood that the interface module 121 may be physically within a station, for example in the form of the Conan integrated circuit or similar network transceiver and associated control software.

As shown in Figure 3, where the interface module 123A is provided as one function within a radio cassette player 103 having also amplifier 310, tuner 312, tape playback deck 314, audio/video controller (AVC) 316 and user I/O 318 functions. These functions and their interconnections are not shown and have no direct bearing on the present invention. Their implementation will be readily apparent to those of ordinary skill in the art.

Figure 4 is a schematic representation of an interface module (in this case node 121) linking a station to the known fibre optic ring. All stations connected to the LAN can generate and/or receive source data and control data. The control data is of low volume, arrives in burst and is user/event driven (eg user instructions or status changes), whereas the source data is a continuous high volume stream (eg audio, compressed video, CD-ROM data).

D2B Optical Frame Structure

In the known D2B Optical system, the source data and control messages are transported on the network from node-to-node in frames generated by the System Master. Frames are circulated at the same rate as the audio sample frequency, typically f_s = 44.1kHz. Frames are grouped into blocks of 48 frames.

Figure 5 shows how each D2B Optical frame is divided into two subframes (`left' and `right'). At f_s = 44.1kHz, there will be 88,200 subframes per second. The left subframe is always the first of the pair transmitted on the network. At the physical level, bits are transported with bi-phase encoding. The relationship between the block, frame, subframe and control frame is shown in Figure 5.

Figure 6 shows how each subframe contains 64 bits, handled within Conan as 8 byte fields. The fields comprise the preamble, the transparent channels, 6 bytes of source data, and 8 control/status bits which make up the control frames and the SPDIF status bits. The meaning of the various field will be described in more detail in relation to the D2B Optical Plus protocol. Further detail is also available within the Conan Data Sheet referred to above.

D2B Optical Plus Transceiver

Figure 7 shows in more details a proposed transceiver integrated circuit, implementing the D2B Optical Plus protocols. It should be appreciated, however, that the block diagram illustrates the functional units of the transceiver, and these can be implemented in a number of ways. For example, the transceiver functions can in principle be implemented entirely or substantially by programming of a sufficiently powerful micro-processor, rather than by hardware. In the present implementation, the functions are implemented by special hardware controlled by a RISC processor running under control of a program stored on chip.

Electrical signals received from the optical fibre are detected, decoded and buffered by a network receiver block. Similarly a network transmitter block is provided to drive the optical transmitter for the next segment in the ring. All communications between one station and its neighbouring stations in the ring therefore effectively pass in serial form through the pins RX and TX. Four ports SR0-SR3, are provided for source data in serial format to be provided to the transceiver for transmission via the network. Similarly, source data outputs SX0-SX3 are provided for source data recovered from the network to be supplied to the various functional units of the apparatus in question. Between the network receiver and transmitter and the various source data ports, a source data router allows control over the routing of source data throughout the network and internally of the present station.

The entire network is synchronised with itself and with the sample rate of source data (when active), by means of the master station clock and the phase locked loop (PLL) working in the transceiver of each station. In particular, the PLL at each station around the ring recovers the serial data clock from the network signal at pin RX and generates timing signals for control of the apparatus, and for onward transmission at pin TX. For functioning as a master station, a crystal oscillator is provided. The clock manager comprises counters and registers suitable for adapting the functions of the entire circuit to different data rates, and for generating clock signals appropriate to other components within the device. An audio synchronising unit provides clock signals to external audio signal processing circuitry, such as a CD player mechanism. In the case where, for example, a digital audio broadcast is to be received, the audio synchronising unit may receive clock signals to act as the master clock for the entire network.

A speed control pin provides input to the clock manager, for use in providing compatibility with D2B Optical networks in a manner to be described hereinafter.

Finally, within the transceiver, a control unit provides various interfaces for microprocessor control of the network transceiver. Standard serial interfaces I2C/SPI are provided for serial control. A novel parallel interface provides for parallel control functions and/or source data output. Within the control unit, various functions and options within the transceiver are controlled and reported to the controlling microprocessor (not shown) via a number of dedicated registers, in a conventional manner. A control port provides access to the transparent channels of the D2B Optical/D2B Optical Plus network.

The function of each pin is specified in Table 1 below.

Table 1

Pin Name	I/O	Function
/RST	In	Reset (active low)
RMCK	Out	Received Master Clock
PLL_LOCK	Out	PLL Lock Indicator
STB	Out	Start of Block
SPEED_CON	In	Conan/Super Conan Speed Select
VDDP	In	Power Rail - Digital IO Pads(+5V)
VSSP	In	Ground - Digital IO Pads
XTO	Out	Crystal Out
XTI	In	Crystal In
P_S0	In	Parallel/Serial Interface Select 0
P_S1	In	Parallel/Serial Interface Select 1
VREF	In	PLL Voltage reference (and reset timing)
FILT	-	PLL Loop filter
VSSA	In	Ground - Analog
VDDA	In	Power Rail (+5V - Analog)
RX	In	D2B Network Receive
ERROR	Out	Error Indicator
TX	Out	D2B Network Transmit
VSS2	In	Ground - Digital Core
VDD2	In	Power Rail - Digital Core (+5V)
MP_WAIT	Out	Wait Output from Parallel Interface
D0-D7	In/Out	Bi-directional Data Bus between processor and PI
A0-A3	In	Input Address Bus to Parallel Interface .
P_CLK	In	Microprocessor Clock for PI
/MP_RD	In	Input read strobe to PI (active low)
/MP_WR	In	Input write strobe to PI (active low)
/MP_CCS	In	Input chip select to PI (active low)

PKT_IN	In	Packet Input Flag
PKT_OUT	Out	Packet Output Flag
CS_AD1	In	SPI Chip select or I2C address select
SDIN_AD0	In	SPI data in or I2C address select
SCL	In	I2C and SPI Clock
SDOUT_SDA	In/Out	SPI data out or I2C data
/INT	Out	Interrupt Output (open drain)
SR0	In	Source Data Input Port 0
SR1	In	Source Data Input Port 1
SR2	In	Source Data Input Port 2 or High Speed Data Input
SX0	Out	Source Data Output Port 0
SX1	Out	Source Data Output Port 1
VDD1	In	Power Rail - Digital Core (+5V)
VSS1	In	Ground - Digital Core
SX2	Out	Source Data Output Port 2 or High Speed Data Output
SER_IN1	In	Transparent Port Input 1
SER_OUT1	Out	Transparent Port Output 1
SER_IN0	In	Transparent Port Input 0
SER_OUT0	Out	Transparent Port Output 0
FSY	In/Out	Frame Sync
SCK	In/Out	Shift Clock
TCCLK	Out	Transparent Channel Clock Out

The new transceiver is designed to allow inter-operability with existing D2B Optical products constructed around the Conan D2B Optical interface device (C&C Electronics Part Number OCC8001), while allowing higher data rates if wanted. A comparative list of the key performance benefits of the new transceiver compared to Conan is as follows :

Source data rate is increased from 4.2336 to 9.867Mbps (or 10.57Mbps if using High Speed Mode for Source Data).

The number of Serial Source Data Channels accessible from each interface transceiver is increased from 3 to 4.

The D2B Optical clocking and synchronisation mechanisms (master-slave sync using PLL) are maintained with no additional connections.

The new transceiver provides the ability to select between Serial interface such as I2C/SPI or standard Microprocessor 8-bit Parallel Interface for control data as well as a total of 4 source Ports (SR0 to SR3) for serial or Parallel Interface. The data rate of the I2C control port is increased to 400 kHz and that of the SPI control port to 2 MHz.

The frame structure for D2B Optical is maintained whilst doubling the source data capacity. The new transceiver with these features enables networks which mix nodes based on either Conan (D2B Optical) or the new transceiver (D2B Optical Plus) to be constructed, as shown in Fig 12, and described later with reference to Figures 13 and 14.

D2B Optical Plus Frame Structure

Figure 8 shows the relationship between the block, frame, subframe and control frame is D2B Optical Plus. As in the D2B Optical system, the source data and control messages are transported on the network from node-to-node in frames generated by one station designated as the System Master. Frames are again circulated at the same rate as the system sampling frequency, typically f_s = 44.1kHz. Frames are grouped into blocks of 48 frames. The frame is again divided into two subframes ('left' and 'right'). At f_s = 44.1kHz, there will still be 88,200 subframes per second. The left subframe is always the first of the pair transmitted on the network. At the

physical level, bits are again transported with bi-phase encoding.

The primary difference is that each subframe contains twice as many bits (128), with an encoded frequency of 22.5 MHz instead of 11.25 MHz (approx).

D2B Optical Plus Subframe (Normal Speed Mode for Source Data)

Figure 9 shows the new normal speed mode. Each subframe contains 128 bits, handled within the transceiver as 16 byte fields. The fields comprise the preamble, the transparent channels, 14 bytes of source data, and 8 control/status bits which make up the control frames and the SPDIF status bits. The meaning of these fields will be described below.

D2B Optical Plus Subframe (High Speed Mode for Source Data)

Figure 10 shows the D2B Optical Plus subframe structure for a network (or network segment) operating in a special high speed mode for maximum source data capacity. Each subframe still contains 128 bits, handled within the transceiver as 16 byte fields. The fields comprise the preamble 4 Bits, 15 bytes of source data, 2 Control Frame (CF) Bits and Parity Bit. The extra byte of source data is gained by removing the four transparent channel bits and the SPDIF status bits.

Preamble: The preamble synchronises the network receiver. There are three types of preamble, identical to those defined in the IEC-958 (SPDIF) specification. They contain bi-phase coding violations which the receiver can

right and block subframes. The left preamble identifies the beginning of a frame and the block preamble identifies the beginning of a block. The block preamble replaces every 48th left preamble. This provides a block structure to which the control frame data is synchronised.

Transparent Channels: The four TC bits enable the transport of four serial channels for proprietary control or status information on the network, with no additional hardware or software overhead. The use of these channels can be left open to system designers, who must define their own protocols for applications. Typical applications include the transport of raw control or status information, such as RS232-type data, VICS data, GSM data, PIN Card data, etc.

Source Data Bytes: The source data bytes carry the high-volume real-time digital source data. The bytes may be allocated flexibly, so that the devices in a system may use the source data bytes in the most efficient way for that system. The mechanism used for allocating the bytes is described below in the section headed Source Data Routing.

Status Bits: If an SPDIF (IEC-958) channel is being transported (using the ports SR0 and SX0 of the transceiver circuit), the V, U and C bits of the D2B Optical Plus subframe contain the validity, user and channel status bits of the SPDIF channel. The left/right convention of these bits is determined by the left/right preambles. The Start Block bit SB identifies the block boundary of a synchronous SPDIF channel and is set after every block of 192 frames (synchronised with the SPDIF signal that is being transported). This synchronisation is performed automatically by the transceiver chip. The Parity bit P generates even parity for the entire subframe.

Control Bits: The control bits CF0 and CF1 carry the control messages (for controlling devices and sending status information). There are 2 CF bits per subframe, and a control frame is 192 bits long, therefore 96 subframes (48 left + 48 right) are required to build-up a complete control frame. The control frame is shown in Figure 11 and is the same for D2B Optical and D2B Optical Plus segments.

Control Frame

As shown in Figure 11, the control frame is assembled from and aligned with a block of 96 subframes, i.e. the first two bits of a new control frame are taken from the subframe with a block preamble, and subsequent pairs of bits are taken from subsequent subframes to build up a control frame. The control frame is identical to that of D2B Optical, allowing control messages to pass seamlessly between D2B Optical and D2B Optical Plus segments of the network.

The fields of the control frame are:

- Arbitration bits: These indicate if the control frame is free or occupied. The transceiver handles these bits automatically.
- Destination Address: This is the 12-bit device address of the destination of the message, in the range '000'H to 'FFF'H. The sending device writes this into its message transmit buffer for transmission. Certain addresses and address ranges have special meanings.
- Source Address: This is the 12-bit device address of the sender of the message, in the range '000'H to 'FFF'H. The receiving device can read this from its message receive buffer after reception. Certain addresses and address ranges have special meanings.

• Message Type and Length: Two 4-bit fields normally used to indicate the type/length of the message. These bits are transported transparently by Conan.

• Data 0 to 15: The message data. All 16 bytes are always transported. The Message Length normally indicates how many of the 16 bytes are actually valid for the message. The sending device writes this into its message transmit buffer for transmission. The receiving device can read this from its message receive buffer after reception.

• CRC: A 16-bit Cyclic Redundancy Check value used to verify that the control frame has been transported without error. The CRC is generated by Conan automatically on message transmission and checked by Conan automatically on message reception.

• ACK/NAK: Acknowledge and Not Acknowledge (2-bits each) indicate successful message transmission. The use of separate ACK and NAK flags allow reliable point-to-point and broadcast message transport, as described in our application GB-A-2302243. The flags are automatically filled by the destination device(s) (if present) and read by the sending device.

• Reserved: 10 bits are reserved for future definition.

Transceiver Parallel Interface

The key features of the parallel interface (PI) in the novel transceiver are as follows: An 8 bit data bus provides connection to external microprocessors. A 2 by 32 byte internal buffer is provided for read and write to the D2B Optical Plus network. Sustained Source data rates up to 10.584 Mbps (1.323 Mbytes per second) (at Fs = 44.1 kHz) as possible using the 15 byte per frame transfer mode of D2B Optical Plus network. The parallel interface can be used for control data, source data or both under control of external configuration pins (P_S0, P_S1).

Packet based date is automatically accommodated in the source data channel.

Two 32x8 bit on-chip RAMs are used in order to assure a constant interrupt rate, equal to the network "sampling" frequency (50 kHz maximum). The top 16 words in the RAM (A[7]=1) contain source data for the "Right" subframe, whereas the 16 bottom words are allocated to "Left" subframes. Each of these memory partitions are further divided in 4-byte cells, allocated to every source port (SP0, SP1, SP2), if running in Normal mode. In High Speed Source Port mode the whole buffer is allocated to the Source Port 3. The 16th byte (address 01111/11111) is only used in conjunction with packet-based data. In that case, a hexadecimal 0x00 indicates a vacant packet slot (subframe). A 0x01 (or indeed any number whose LSB is 1) will identify a used packet slot.

At any one time, one of the two RAMs is assigned to serve the internal RISC processor of the transceiver, while the other is dedicated to the external microprocessor (not shown). Both the external device and the internal processor have direct access to these memories, by means of a full crossbar 2x2 switch. The RAMs are swapped whenever an interrupt is asserted. This operation is transparent to both the external device and the internal processor.

The external microprocessor communicates to the PI through an interrupt request line, an 8-bit bi-directional data bus, a 4-bit address bus and three registers: STATUS, ADDRESS and DATA. See Table 1 for a summary of those pins associated with the parallel interface PI. An ADDRESS register is used to store the address of the internal register that is accessed. All data is exchanged via the DATA register.

The general operation of the parallel interface is not relevant to the present invention, and will not be described further.

Serial Source Data Formats

To maximise the application versatility of the chip, three serial source data ports are provided. This means that a product which needs to process source data for more than one internal source or destination can do so with only one transceiver chip. These source data ports can transfer 8, 16, 24 or 32 bit source data, left or right adjusted, in to and out of the device.

The source data ports provide access to the source data in the network bit-stream. Data can be input and output serially through seven serial inputs (SR0 to 3) and seven serial outputs (SX0 to 3) or using the Parallel Interface. When in serial mode all seven ports use a common frame synchronisation FSY and a serial bit clock SCK. FSY and SCK may be set as either inputs or outputs, depending on the external hardware. If they are configured as inputs, then the data source(s) must be clocked by RMCK to be synchronised in frequency to the network bit-stream (although not necessarily in phase). A special mode is provided which allows source data Port as SPDIF (SR0/SX0). With the control bits in a Source Data Port Control register, a variety of source data formats can be selected.

Source Data Routing

Like the Conan interface circuit the present transceiver maintains a Routing Information Table (RIT) which determines the connection between the various source data ports and bytes within the source data fields of the D2B Optical or D2B Optical Plus frames.

Figure 13 shows an example of routing through the Routing Information Table in the case where the transceiver is transmitting in D2B Optical format (11.2896Mbps) and receiving in D2B Optical Plus format (22.5792Mbps). Some, but not all active connections are shown by arrows, for clarity.

Figure 14 shows an example of routing in a reverse situation, when a transceiver is receiving from a low speed D2B Optical segment and transmitting to a high speed D2B Optical Plus segment. Again, not all connections are shown by arrows, for clarity.

It will be seen that the RIT has an entry corresponding to each byte field on the "output" side, which includes bytes of the frames being transmitted to the network and bytes output within the network station from the ports SX0-SX2 of the transceiver. The value stored for each entry in the RIT acts as an index to identify the source of the data for the output, which may be a byte field of the incoming network segment, or a byte field from one of the source data ports SR0-SR2.

In the example of Figure 13, two 16-bit stereo signals are input to the transceiver at ports SR0 and SR1, and output to the D2B Optical network segment in bytes D1-D4 (left) and D9-D12 (right) of the network subframes. For other byte wide channels are passed straight through from the incoming network segment to bytes D0, D7, D8 and D15 of the following segment. Two 16-bit stereo channels are retrieved from the incoming network signal and output from the transceiver port SX0.

It will be appreciated that the system described has various novel and useful features, while these various aspects of the invention are in no way limited to the particular embodiments described herein.

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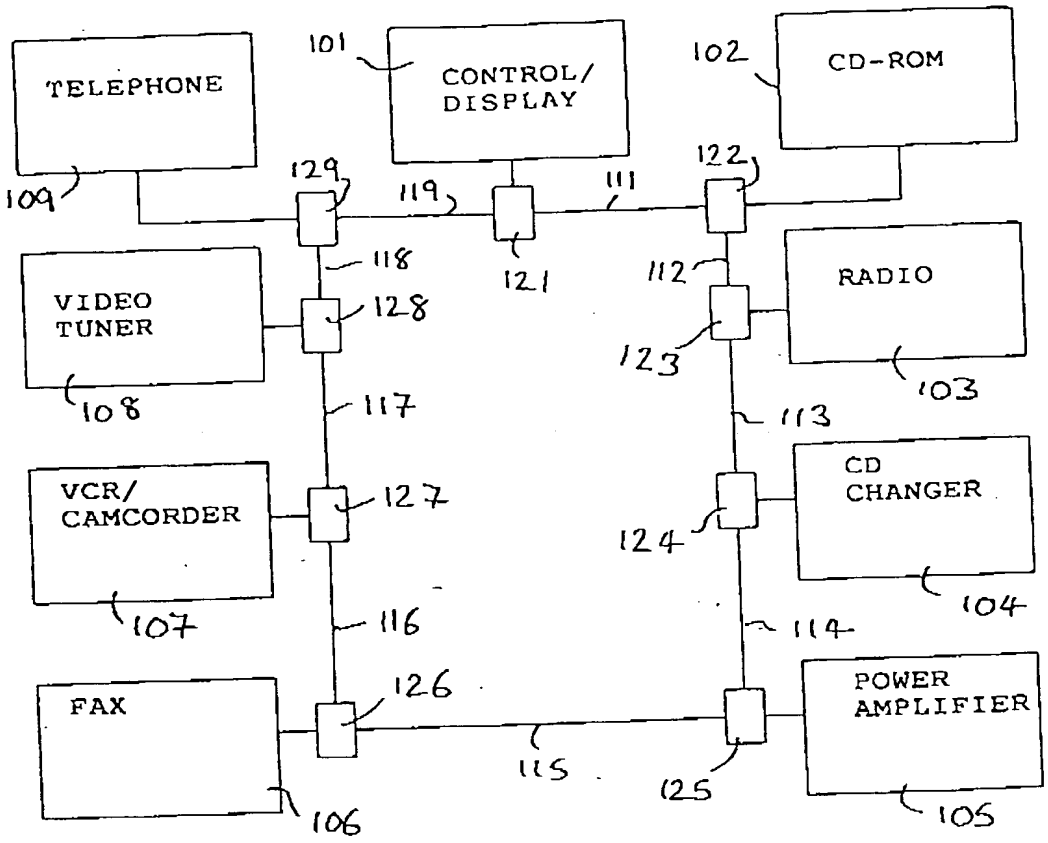
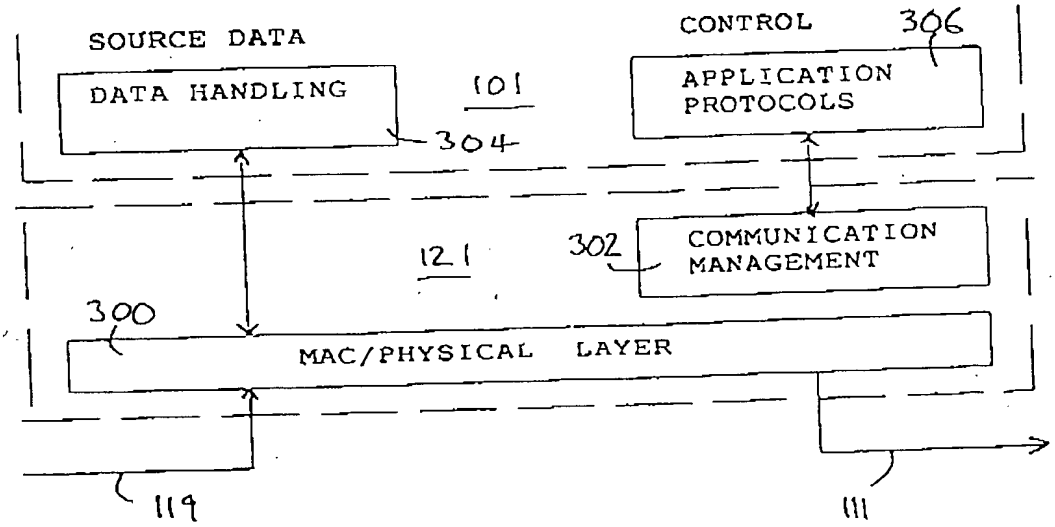


Fig.1 (PRIOR ART)

Fig.2 (PRIOR ART)



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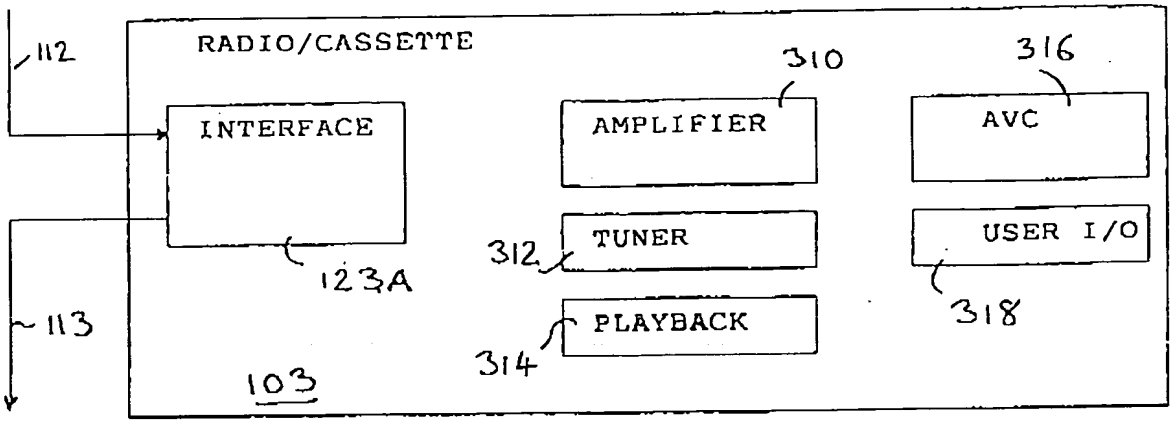

Fig.3 (PRIOR ART)

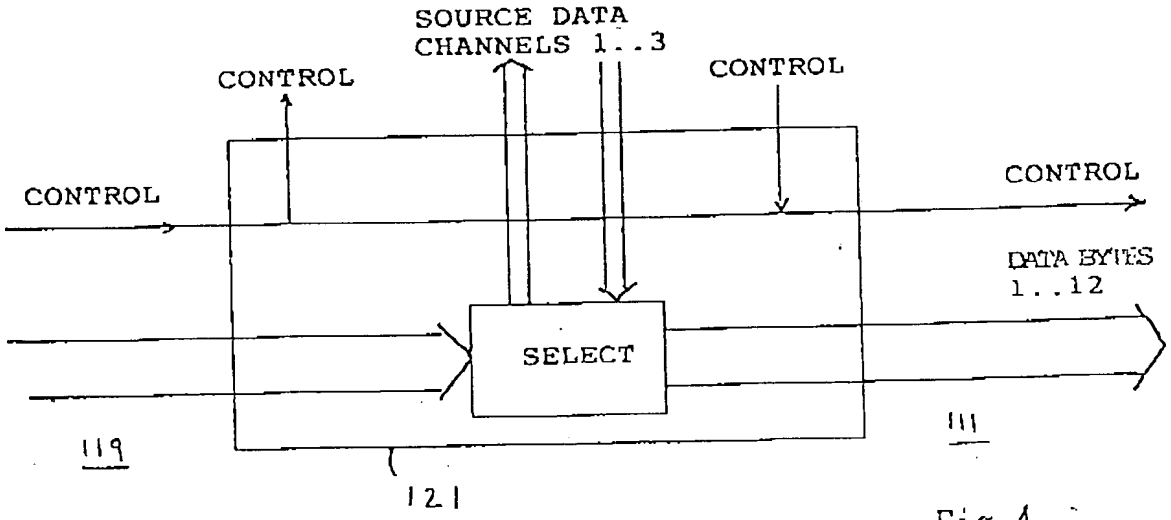

Fig.4

(PRIOR ART)

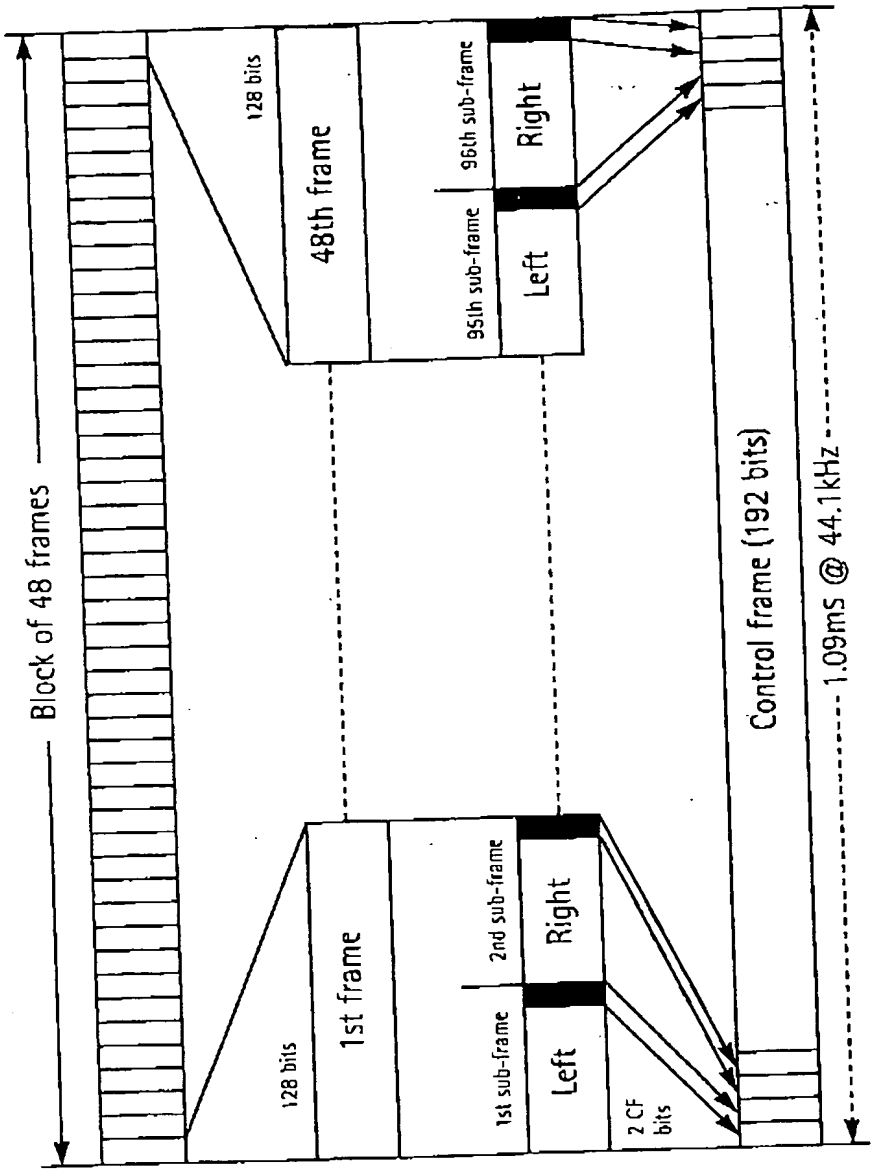

Fig. 5
(PRIOR ART)

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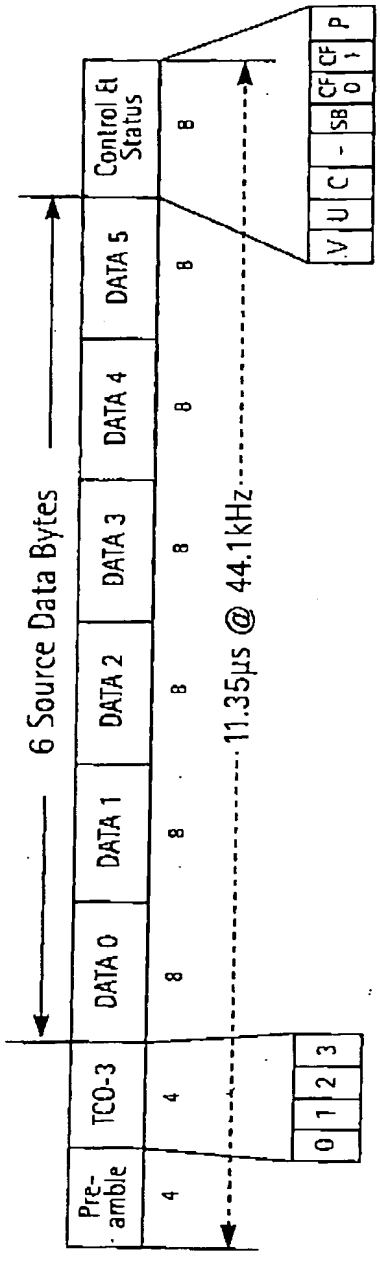

Fig. 6 (PRIOR ART)

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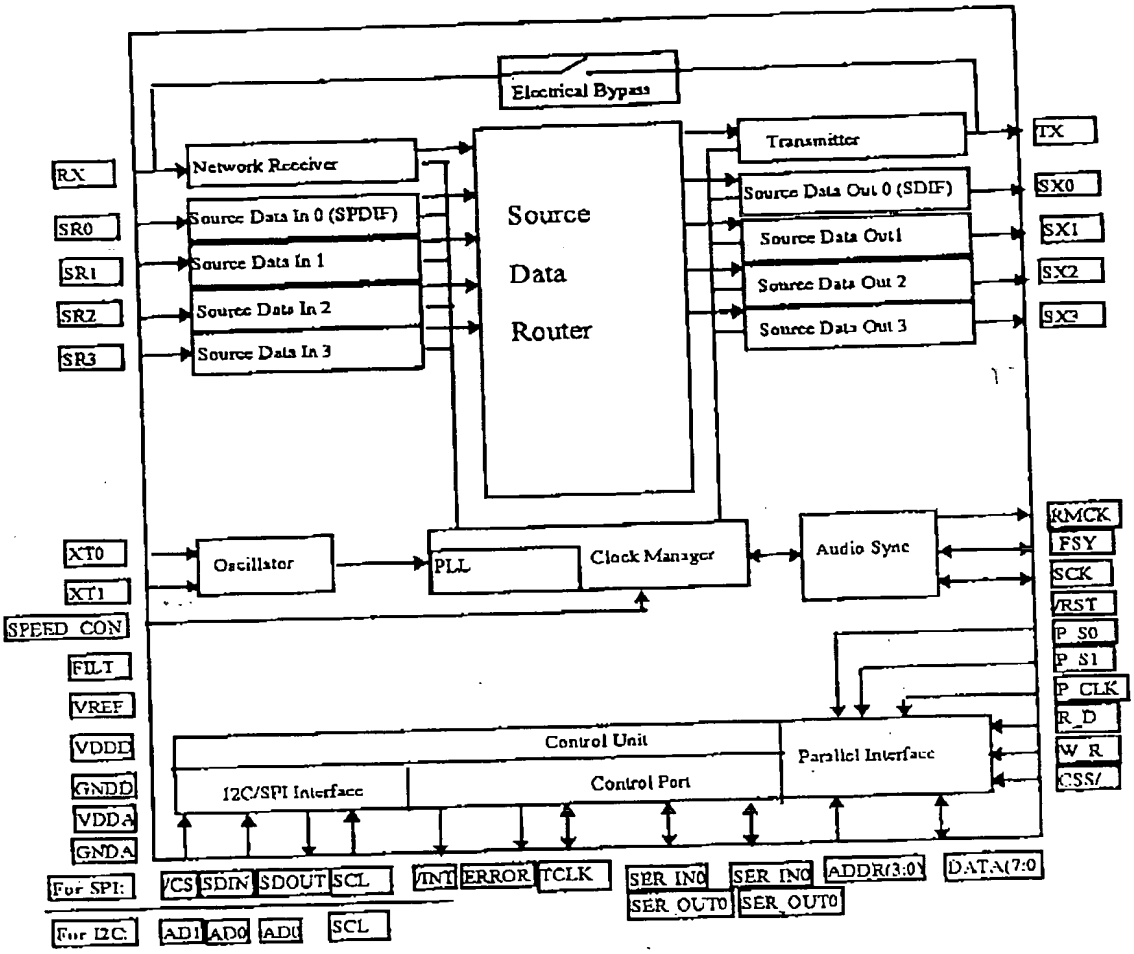
Electrical Bypass
RX
Network Receiver
SR0
Source Data In 0 (SPDIF)
SR1
Source Data In 1
SR2
Source Data In 2
SR3
Source Data In 3
Source
Data
Router
Transmitter
Source Data Out 0 (SDIF)
Source Data Out1
Source Data Out 2
Source Data Out 3
TX
SX0
SX1
SX2
SX3
XT0
XT1
SPEED CON
FILT
VREF
VDDD
GNDD
VDDA
GNDA
Oscillator
PLL
Clock Manager
Audio Sync
RMCK
FSY
SCK
/RST
P_S0
P_S1
P_CLK
R_D
W_R
CSS/
Control Unit
Parallel Interface
I2C/SPI Interface
Control Port
For SPI:
/CS
SDIN
SDOUT
SCL
/INT
ERROR
TCLK
SER_IN0
SER_IN1
ADDR(3:0)
DATA(7:0)
SER_OUT0
SER_OUT1
For I2C:
AD1
AD0
AD0
SCL

Fig. 7

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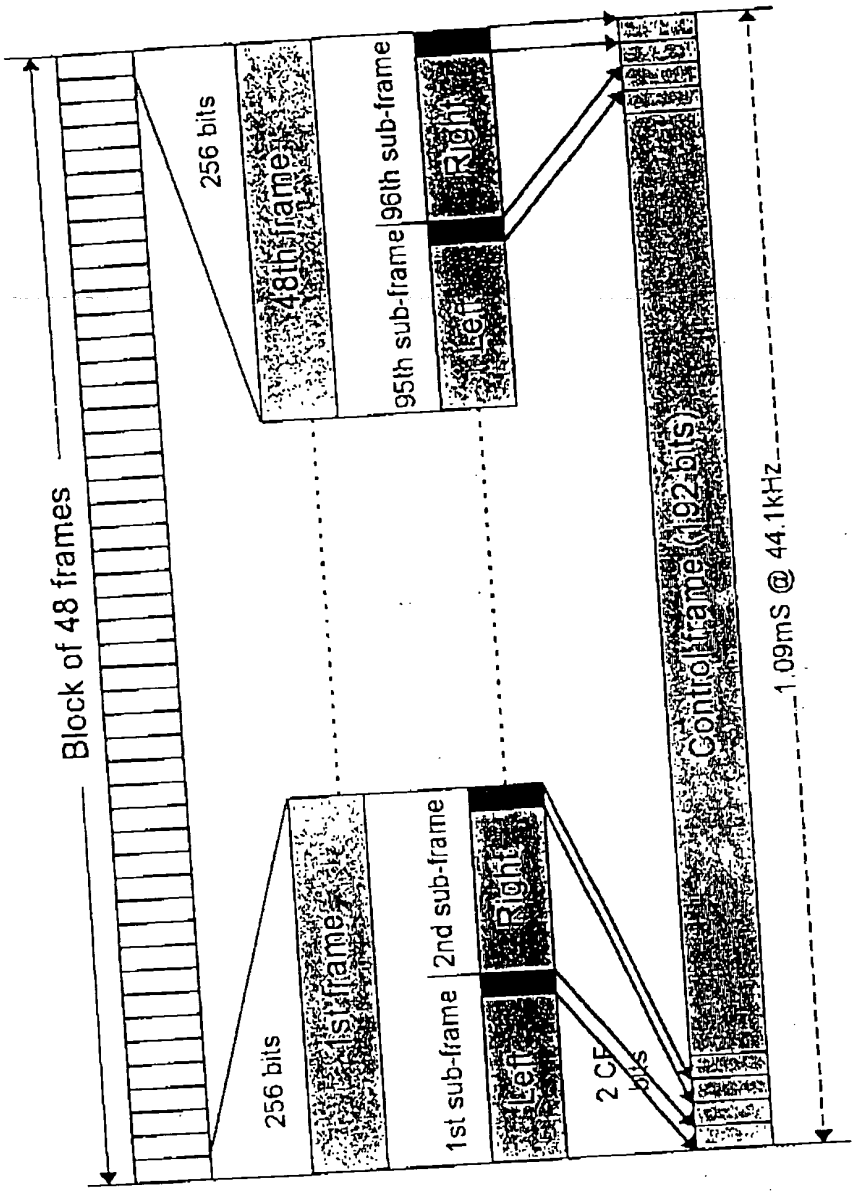
Block of 48 frames
256 bits
48th frame
96th sub-frame
95th sub-frame
Right
Left
1st frame
2nd sub-frame
1st sub-frame
Control frame (192 bits)
2 CF bits
1.09mS @ 44.1kHz

Fig. 8

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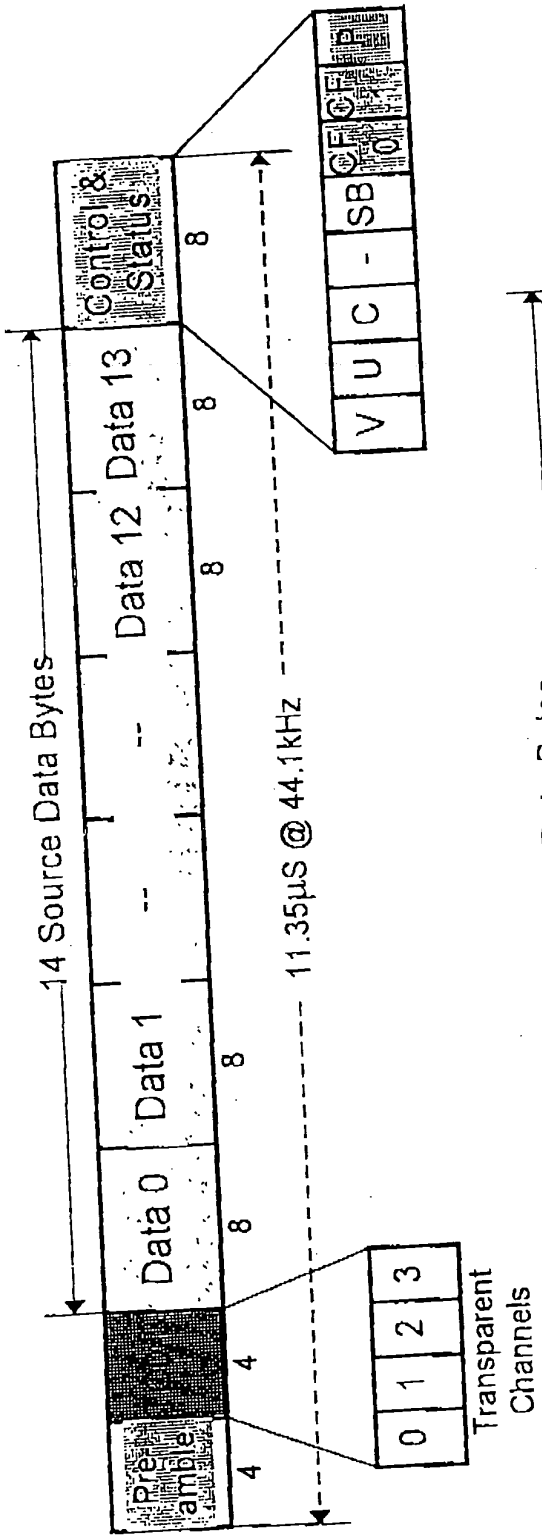

Fig. 9

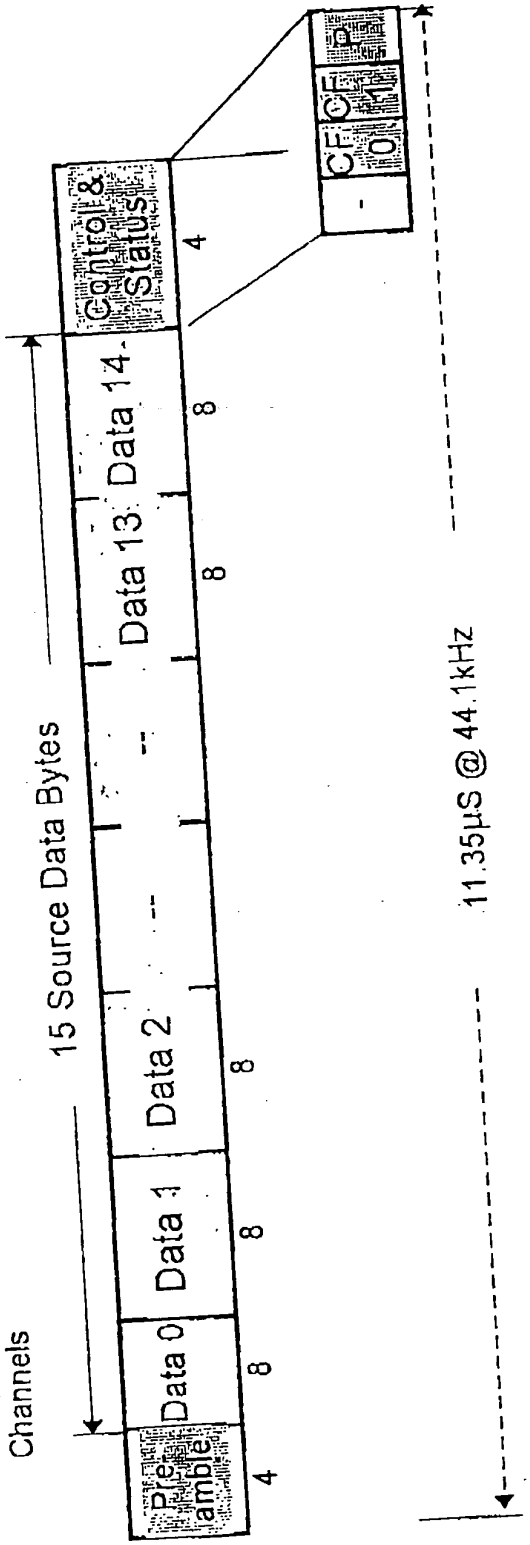

Fig. 10

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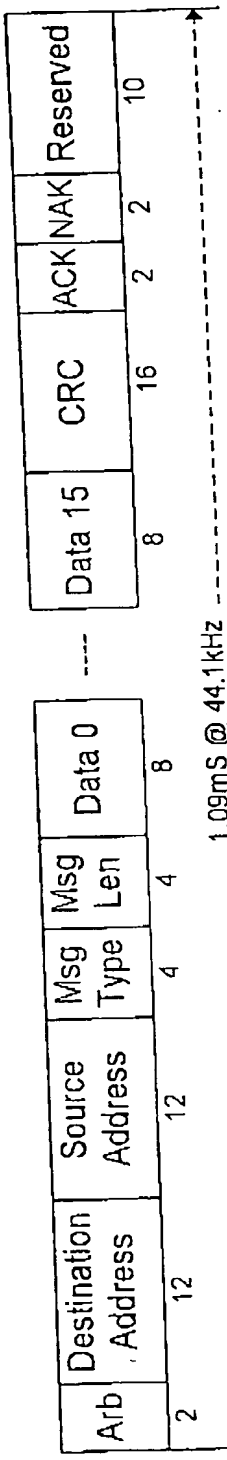
Arb
2
Destination Address
12
Source Address
12
Msg Type
4
Msg Len
4
Data 0
8

Data 15
8
CRC
16
ACK
2
NAK
2
Reserved
10
1.09mS @ 44.1kHz

Fig. 11

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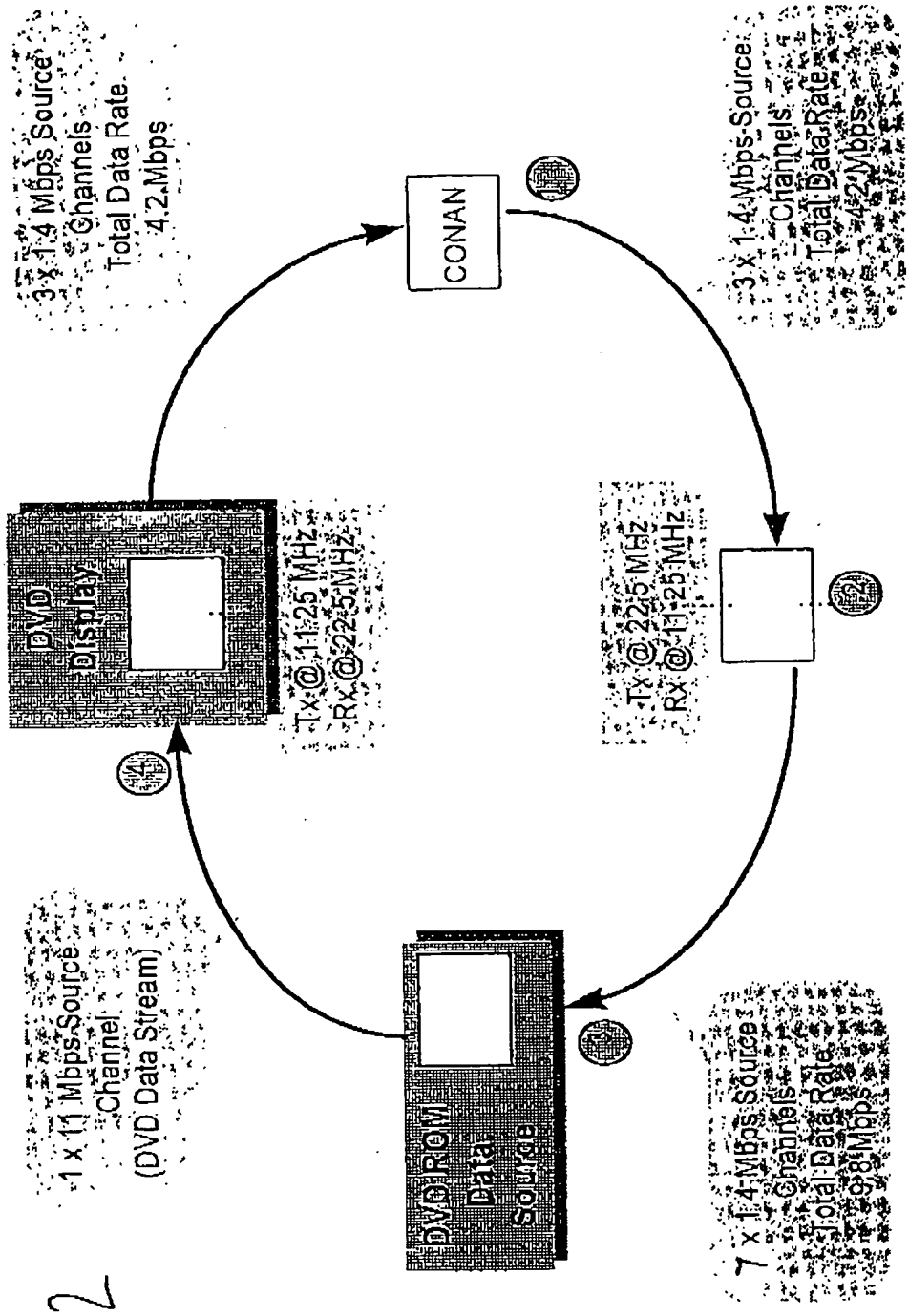
3 x 1.4 Mbps Source Channels
Total Data Rate
4.2 Mbps
CONAN
3 x 1.4 Mbps Source Channels
Total Data Rate
4.2 Mbps
DVD Display
Tx @ 11.25 MHz
Rx @ 22.5 MHz
Tx @ 22.5 MHz
Rx @ 11.25 MHz
1 x 11 Mbps Source Channel
(DVD Data Stream)
DVD ROM Data Source
7 x 1.4 Mbps Sources Channels
Total Data Rate
9.8 Mbps

Fig. 12

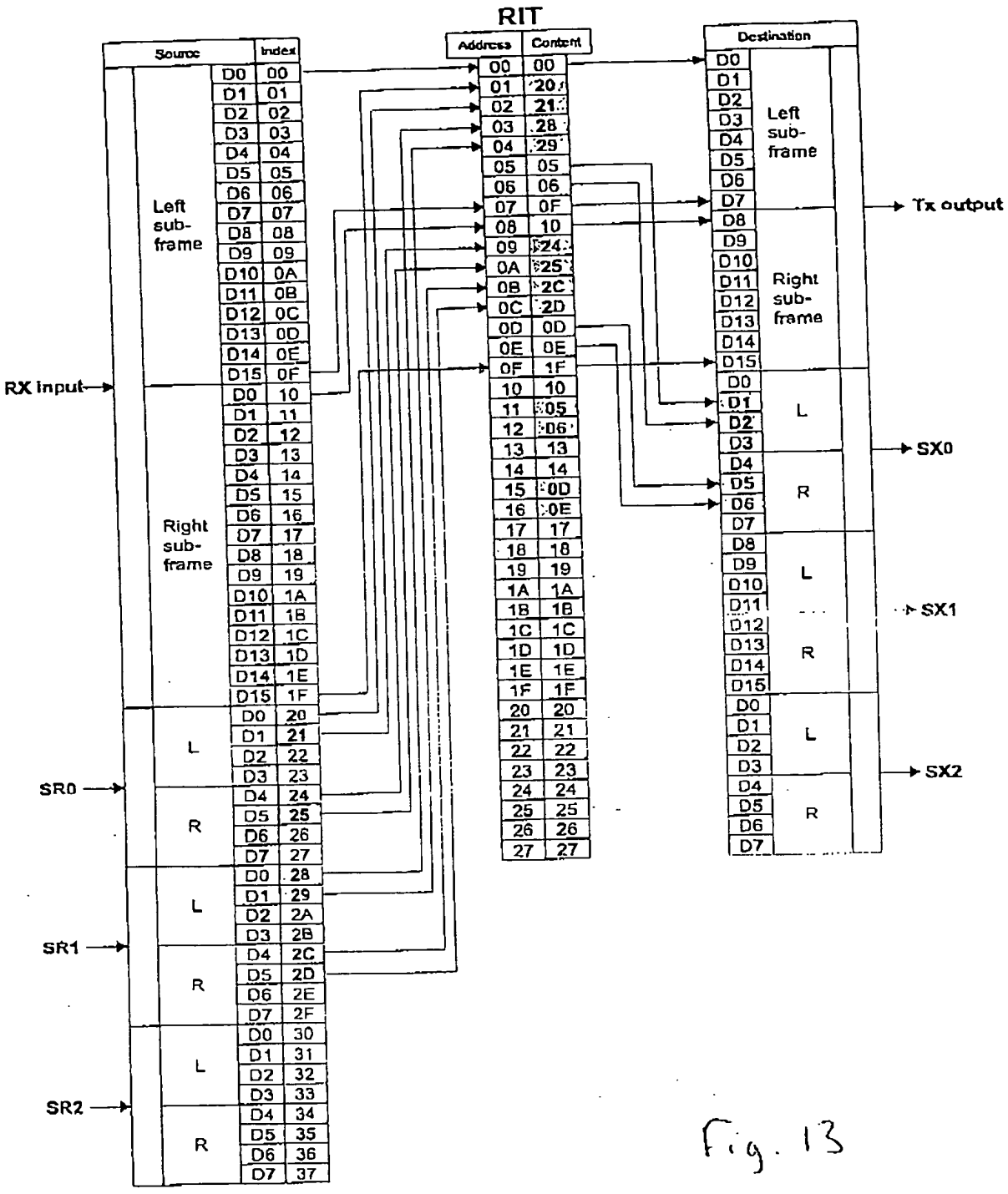
RIT
Source
Index
Address
Content
Destination
Left sub-frame
Right sub-frame
RX Input
SR0
SR1
SR2
L
R
Tx output
SX0
SX1
SX2

Fig. 13

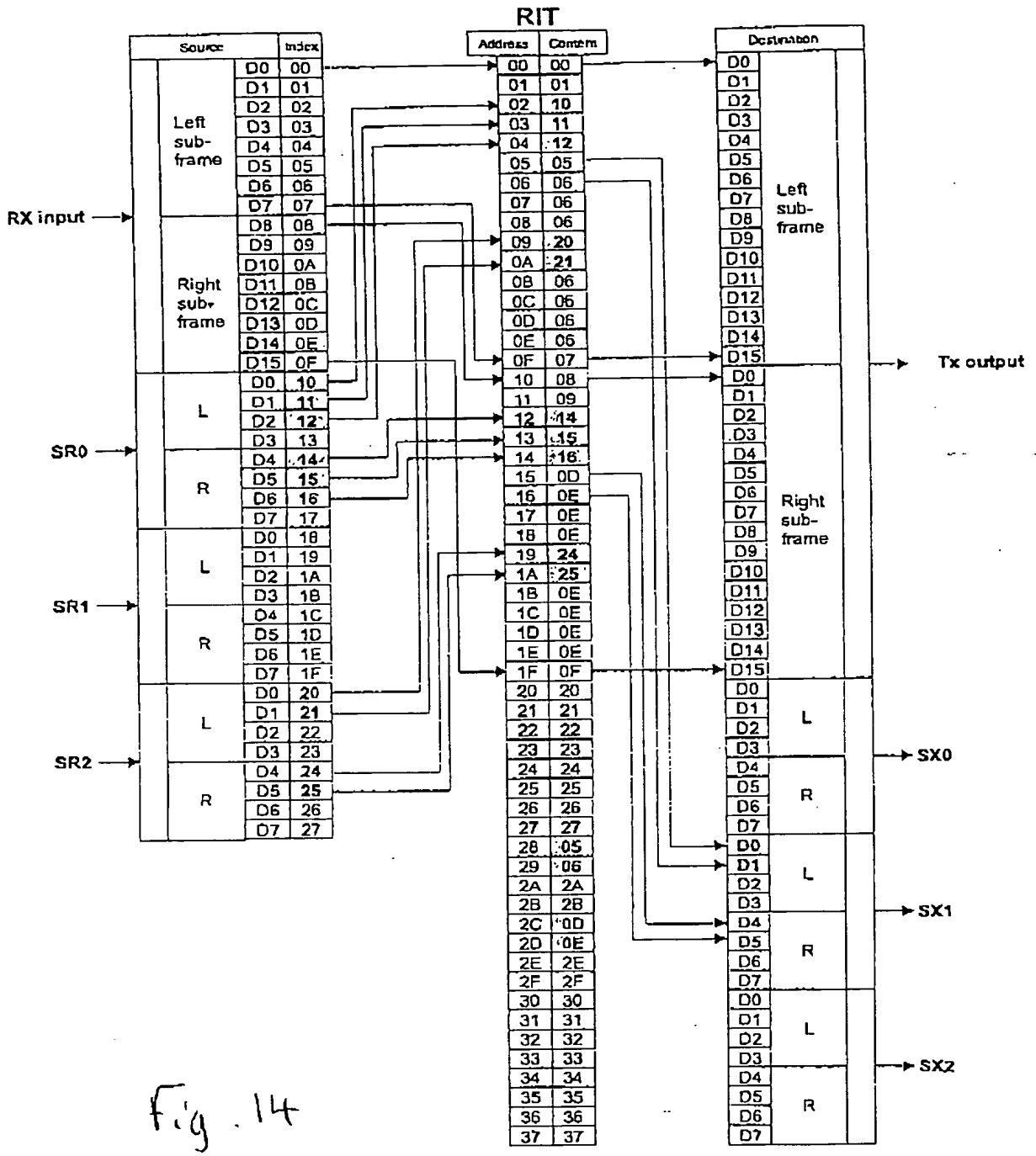
RIT
Source
Index
Address
Content
Destination
RX input
SR0
SR1
SR2
Left sub-frame
Right sub-frame
L
R
Tx output
SX0
SX1
SX2

Fig. 14